Abstract of the Disclosure

A plurality of semiconductor chips (14) each having a first main surface (14b) formed with electrode pads (21) and a second main surface (14c) opposite to the first main surface are respectively mounted on a chip mounting surface (12a) larger in area than the second main surface, of a wafer-shaped mounting substrate (12) at equal intervals so as to extend along first and second trenches (18a, 18b) defined in the chip mounting surface with these trenches as target lines. Thereafter, solder balls (25) electrically connected to the electrode pads of the semiconductor chips are disposed on their corresponding wiring patterns 34 that extend from above first regions (100) located above the semiconductor chips, of a surface region of an encapsulating layer (32) covering the semiconductor chips to above second regions (200) that surround the first regions. Afterwards, the encapsulating layer and the mounting substrate are cut and thereby fractionized into semiconductor devices each having a fan-out structure.